A High-Speed, Time-Division Multiple-Access Communication Link Demonstration

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The development of a demonstration 250-Mbps, time-division multiple-access communication link is presented and test results are reported. To establish this demonstration link, a frame synchronizer, a time-division multiple-access demodulator, and a time-division multiple-access modulator were developed. The prototype system is described with emphasis placed on the test results. Bit error performance, acquisition, characteristics, bit count integrity, and the ability of the station to stay in the network are evaluated. The communication link was designed based on computer simulations. The correlation between the test results and the analytically predicted performance is discussed. Test results indicate that a communication station will not disturb the time-division multiple-access network at any signal-to-noise ratio; however, there is a minimum signal-to-noise ratio below which the stations's ability to remain continuously in the network is impaired.

Nomenclature

A/D	= analog-to-digital
AFC	= automatic frequency control
ALC	= automatic level control
AW	= Advanced Westar
BER	= bit error rate
BPF	= bandpass filter
CW	= continuous wave
E_b	= signal energy per data bit
EOB	= end of burst
HPA	= high-power amplifier
LNA	= low-noise amplifier
N_0	= equivalent noise power in ideal filter matched to the data bit
PLL	= phase-lock loop
RS	= reference station
RSS	= reference station simulator
RUW	= reference unique word
SIC	= station identification code
SQPSK	= staggered quadraphase shift keying
TDMA	= time-division multiple-access
TDRS	= Tracking Data and Relay Satellite
TSA	= transmit slot acquisition
UW	= unique word
VCXO	= voltage controlled crystal oscillator

Introduction

AMONG the first satellites to be deployed by the Space Shuttle is the Tracking Data and Relay Satellite (TDRS). This satellite contains two payloads and can operate in one of two configurations, TDRS or Advanced Westar (AW). The AW payload is divided into a C-band and a Ku-band system. The Ku-band payload provides the first available spacecraft switched time-division multiple-access (TDMA) communication network in the United States.

The Advanced Westar System has a 1 Gbps information transfer capability. Four simultaneous 250 Mbps transmissions can be supported by the spacecraft, subdividing the 48 contiguous states into four zones. A TDMA switch permutes the receive/transmit routing to provide total interconnectivity between the four zones. The related permutation is repetitive at the 750 μs TDMA frame rate. The satellite switch is free-running; therefore, a reference station (RS) tracks this switch and distributes system timing, which is essential for network synchronization and operation. To operate the network in case of an RS outage, at least two such RSs are needed. Without any timing information, the TDMA demodulator reconstructs the baseband data from the received carrier, and the unique word (UW) detector processes these data to identify the RSs—primary and/or secondary. After the correct reception of the reference burst, receive timing information is available to the Earth station. Based on this timing information and the TDMA network's timing assignment, a synchronization unit issues timing gates to the demodulator, further improving demodulator performance. Under the direction of the synchronization unit, time-slot acquisition (TSA) is initiated. The TSA acquires transmit timing information from knowledge of when the received loop-back burst has to arrive relative to the received reference burst.

Transmit time synchronization is achieved by the measurement of the round trip transmission delay utilizing continuous wave (CW) bursts significantly below the communication signal level. These data, together with the already obtained received timing information, are sufficient for TDMA transmission to commence. Upon completion of this process, the synchronization unit initiates TDMA transmissions. In steady-state operation, the synchronizer tracks loop-back transmissions and adjusts them in small increments at time intervals slightly exceeding the round trip transmission delay. The station's timing relative to the reference UW remains as specified, thereby ensuring network synchronization. Demonstration link showed this design to be operational. In particular, it demonstrated that a station can enter the network at a normalized signal energy-to-noise power ratio (E_b/N_0) as low as 7 dB, and retain synchronization to significantly lower E_b/N_0.

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Design Concept

To demonstrate the AW operational concept, a prototype Earth station was designed (Fig. 1) operating at 250 Mbps. A large number of new design and hardware concepts were developed which fall into either high-speed synchronization unit development or high-speed TDMA modem development.

In the prototype system, a dual reference station simulator (RSS) was built and mechanized to transmit the primary and secondary reference burst anywhere in the TDMA frame. These bursts provide system timing. To simulate operational deployment effects, the primary and secondary RSs can be made to drift relative to one or the other, by as many as four symbols, and can be individually turned off/on. This RS provides periodic frame markers to each station in the AW network. The primary and secondary RS markers are differentiated from each other by station identification codes (SICs).

The AW synchronization concept relies on the detection of a reference unique word (RUW). A 20-symbol (40-bit) RUW is selected with autocorrelation properties guarding against false correlations with a one-, two- or three-symbol displacement. Periodic detection of the RUW maintains each active station synchronized to the RS. This process ensures that each station is synchronized to the AW satellite and to each other.

False acquisitions are avoided by requiring 100% correlation between the received and stored UWs at initial acquisition. Once periodicity is demonstrated with this criteria, steady-state operation is entered. In this mode, the detection criteria are lowered by accepting 6-bit errors in the 40-bit word. The design goal for the AW network was to operate down to an $E_b/N_0 = 6.9$ dB. Analysis shows that accepting less than total correlation in the UW helps toward achieving this goal, but it is not sufficient by itself. To satisfy the operational requirement, an algorithm was devised that requires only one UW detection out of every seven received. In the absence of a detected unique word, the synchronization unit continuously generates a frame marker. To reduce system jitter, the frame marker timing is corrected by up to one symbol at every valid UW detection, similar to a concept developed independently by Acampora and Curry.[1]

The high-speed UW detector and the frame synchronizer hardware perform the function of tracking the RS. Other high-speed synchronization functions include assembly of the preamble, establishment of symbol synchronization for each received burst, and detection of the station identification code, bit error-rate (BER) pattern, order wire, and the data portion.

To ease the requirements on the overall network, successive bursts originating from different transmitters are not coherent. For this reason, the synchronizer establishes symbol coherency in real time for every burst by correlating to the UW in the sequence shown in Fig. 2. Most of the hardware difficulties associated with this task are speed related since, in a TDMA system, clock jitter forces the digital units to operate at effective speeds well in excess of the baud rate.

In addition to requiring complex synchronization hardware, a 250-Mbps TDMA communication system requires a modem design that significantly differs from the designs utilized in CW communication links. To utilize the high system efficiency potential of TDMA communication systems, coherency is required between successive bursts or rapid acquisition is required. In developing this system, cost constraints eliminated coherency between bursts, resulting in unconventional demodulator requirements. Hang-up properties of phase-lock loops (PLLs) eliminate their utilization in both high-speed TDMA carrier and symbol timing recovery schemes.[2] In this design, both the demodulator and the bit synchronizer utilize a high-Q, single-pole cavity filter as the principal aid in carrier and symbol timing recovery, respectively. A single-pole cavity is selected to reduce the response time for a given noise bandwidth, and to increase the stability of the automatic frequency control (AFC) loop utilized for carrier recovery. To further reduce guard times and preamble length requirements, filter quenching is introduced between bursts.

Other requirements to consider in TDMA demodulator design include: large duty factor variations, lock-point ambiguity elimination, and preamble design. The carrier is always present in continuous duty cycle communication links, which greatly simplifies automatic level control (ALC) and AFC loop designs. In a TDMA system, the portion of time during which a signal is present can vary by a factor of 1000. When a single reference station is present, the duty cycle approaches 0.001, while a full-up system is utilized in excess of 90% of the time. Conventional systems, where cycle slipping is not a problem, can resolve the lock-point ambiguity of the receiver utilizing seconds to do so. At 250 Mbps, this TDMA system is allocated a 0.480×10^{-6} s preamble for acquisition. During this time, lock-point ambiguity is eliminated or the BER penalty of differential en-

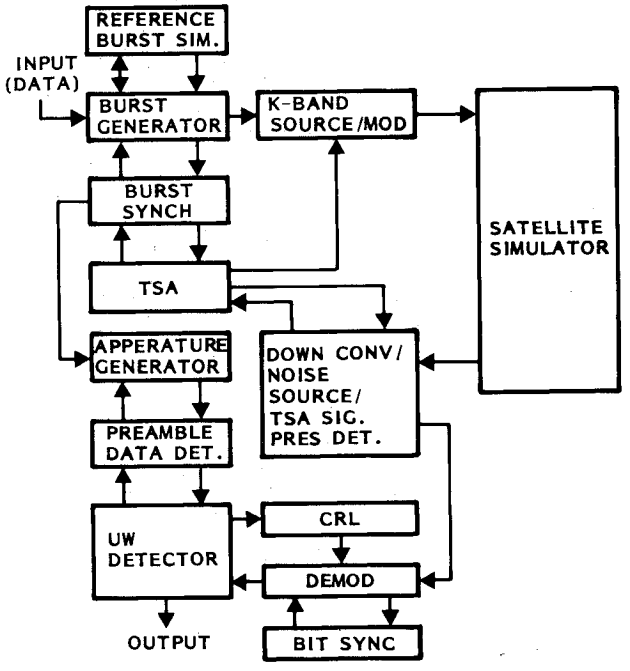

Fig. 1 AW TDMA prototype Earth station.

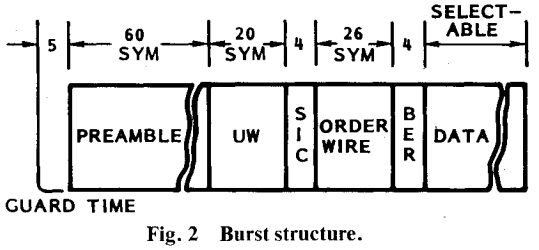

Fig. 2 Burst structure.

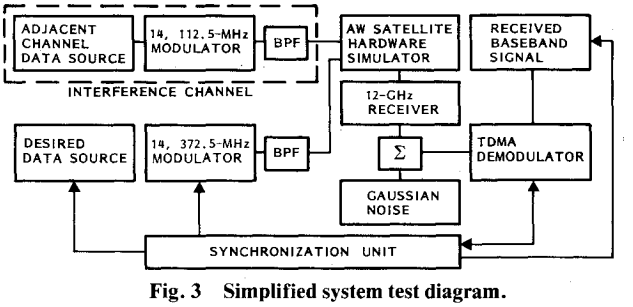

Fig. 3 Simplified system test diagram.

coding is accepted. The corresponding circuits are designed to achieve a 60-symbol preamble for carrier and symbol timing recovery. In addition, the preamble structures are optimized to minimize the impact of combined carrier and bit synchronizer phase error on BER.

Hardware Description

Figure 3 shows the system test configuration. The transmit portion of the AW Earth station is built with high-power amplifiers (HPAs). On the receive side, the low-noise amplifiers (LNAs) are omitted from the link. The transmit and receive stations are linked by an AW satellite hardware simulator. This unit was built to the same electrical specifications as the AW satellite, utilizing many of the engineering model assemblies and units.

The test configuration is that of an RF satellite link with noise added to the receiver to evaluate BER. Because the AW satellite system will operate in TDMA mode, the modulator, data generator, and demodulator, as well as the data transmitter and receiver, operate under the control of the synchronization unit. The AW satellite utilizes a 500-MHz spectrum at Ku-band. Each communication channel is allotted 225 MHz with a 50-MHz guard band between them.

The desired and interference channels typically reach the satellite (in the test case, the AW satellite hardware simulator) with equal power. In such cases, the spectrums are sufficiently separated and little in-band interference is observed. The out-of-band interference is rejected by the satellite's diplexer. However, severe rain attenuation can affect the desired signal without affecting the adjacent (interference) channel. Software simulations show that adjacent channel interference will significantly degrade communication performance unless filtering is used at the output of the transmit Earth station. To confirm these claims, the system test bed was set up with an adjacent interference channel.

To simulate the actual operating conditions of one RS drifting relative to the other (due to changes in orbital geometry and imperfect frequency sources), the dual-reference burst simulator simulates asynchronous frequency drift between the primary and secondary unit. To further simulate the operational system, the data-generating station utilizes an independent clock relative to the reference simulators.

Modulator

The modulator is implemented at Ku-band. This approach allows a significant portion of the system concept to be tested at modem level. More specifically, with a Ku-band modulator the phase noise at modem level can be made similar to that at system level, and wideband thermal noise can be introduced at the modulator simulating the interburst noise characteristics of the AW satellite. As shown in Fig. 4, the modulator accepts separate clocks for the I and Q channels, together with the I and Q data. Carrier suppression is measured by comparing the unmodulated carrier power to the energy in the carrier when quadraphase is modulated by pseudorandom bit streams.

Demodulator

The demodulator unit receives an incoming TDMA staggered quadraphase shift keying (SQPSK) signal, centered at approximately 1.2 GHz, and supplies two output channels of baseband data at 125 Mbauds each. The selected approach shown in Fig. 5 consists of demodulation with a remodulation loop using a single high-Q resonator to enhance the signal-to-noise ratio of the recovered carrier. The design also includes AFC for the recovered carrier and a high degree of tolerance to input frequency offsets. Symbol timing recovery is accomplished by a ringing filter, which is also quenched at the end of each burst. Unambiguous phase detection is achieved by preamble-aided acquisition, allowing identification of only one of the four stable lockup points associated with four-phase remodulation.

The SQPSK RF input signal is first downconverted to 680 MHz. The local oscillator frequency for the downconversion is generated by a voltage controlled crystal oscillator (VCXO), controlled by the error voltage generated in the AFC. The downconverter has two outputs: one feeds the TSA unit, and the second feeds a power divider which in turn feeds the I-Q detector and remodulator via a delay line. This delay line equalizes the normal delay of the baseband signal arriving at the remodulator to cause modulation stripping (wipeoff technique) of the delayed SQPSK signal. The modulator output becomes the reconstructed carrier that provides the signal to the automatic frequency control. The AFC loop is required because the satellite frequency generates uncertainty at the demodulator input in excess of 100 kHz. The reconstructed carrier is filtered by a high-Q bandpass filter (BPF) centered at 680 MHz. The BPF is incorporated into the AFC loop to avoid BER degradation due to filter center frequency offset. The filtered carrier is phase compared with the unfiltered carrier, thus generating an error signal proportional to frequency offset. By this means, the demodulator BER performance remains invariant over a 4-dB input power change. The error voltage generated in the AFC phase detector is fed to the sample-and-hold which is followed by a low-pass filter. This subassembly then supplies the control voltage to the VCXO to maintain proper carrier frequency in the AFC loop. The energy stored in the high-Q BPF is quenched at the end of each burst (EOB); this event occurs at the same time as the remodulator becomes disabled by the enable logic subassembly. The filtered reconstructed carrier feeds the I-Q detector via a phase adjust trimmer. The entire process of remodulation and demodulation is completed by the enable logic subassembly, which allows the remodulator to become active upon proper commands processed by the logic control subassembly. The analog baseband outputs of the I-Q demodulator are power divided to feed the enable logic subassembly and a wideband dual dc amplifier. A hard

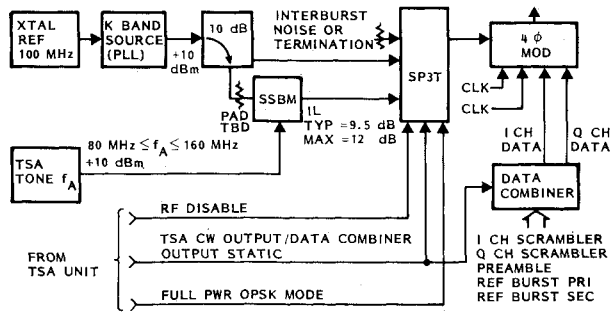

Fig. 4 High-speed TDMA modulator block diagram.

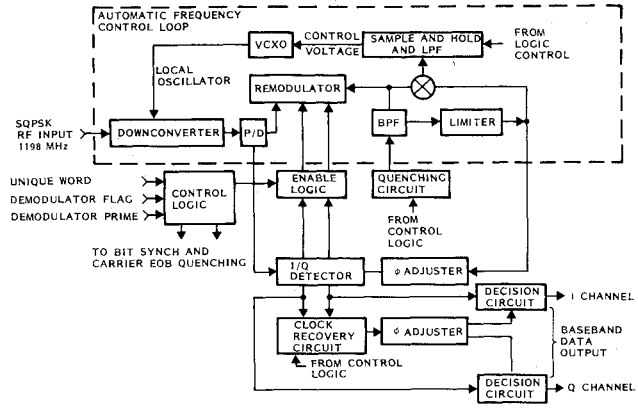

Fig. 5 Demodulator and bit synchronizer simplified block diagram.

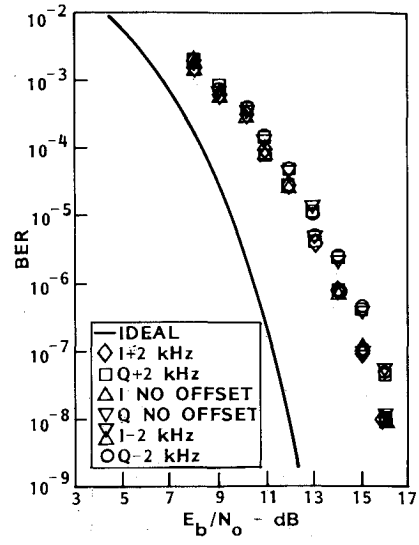

Fig. 6 Degradation to bit error rate, function of clock frequency offset.

decision circuit receives the analog baseband signals and two independent adjustable 125 MHz clocks to generate the output baseband logical data for the I and Q channels; alternatively, a 3-bit analog-to-digital (A/D) converter is available for further processing of the recovered data.

The symbol timing recovery subassembly receives baseband logical data from the enable logic subassembly. These signals are detected by a pair of square law detectors and then summed to generate a 125-MHz symbol timing. A high-Q resonator improves the E_b/N_0 and the ringing effect ensures against amplitude fadeout. The output from the symbol timing recovery feeds a limiter chain to remove amplitude modulation and increase the dynamic range of the preceding subassembly. A pair of manually adjustable phase trimmers follows the limiter chain. The high-Q resonator of the symbol timing recovery is also quenched at the end of each burst by a control command. The control logic subassembly receives digital signals from the electronics acquisition unit and processes them to suitable commands for the demodulator unit.

Synchronization Unit

Because the satellite switch is free-running, an RS tracks this switch and distributes system timing, which is essential for network synchronization and operation. To protect the network in case of an RS station outage, at least two RSs are needed. In the prototype system, a reference burst simulator serves as a dual RS. It generates both primary and secondary reference bursts, providing system timing. To simulate satellite-induced Doppler and source instabilities the two reference bursts drift relative to each other, as specified by the operator. These signals are modulated at Ku-band and routed to the receiver where they are downconverted to the demodulator's input frequency and passed through an ALC unit. Without any timing information, the TDMA demodulator reconstructs the baseband data from the received carrier, and the UW detector possesses this data to identify the RSs as primary and/or secondary. After the correct reception of the reference bursts, receive timing information is available to the Earth station. Based on this timing information and the TDMA network's timing assignment, the aperture generator issues timing signals to the demodulator, improving demodulator performance. The aperture generator also gates the UW detector and TSA unit.

To limit false acquisition after system timing has been established, the UW detector is gated to a ± 3 symbol uncertainty. UW correlation, in turn, establishes bit timing; therefore, the UW detector gates the preamble generator to examine the four symbols of station identification code, 26 symbols of order wire, and in the case of loop-back transmission, four symbols of BER. Under the direction of the aperture generator, TSA is initiated. The TSA acquires transmit timing information from the knowledge when the received loop-back burst has to arrive relative to the received reference burst.

Transmit time synchronization is achieved by the measuring of the round trip transmission delay using CW bursts, nominally 25 dB below the communication signal level, and adjusting the transmit timing by the round trip delay so that the loop-back burst falls into the established timing window. Upon completion of this process, the burst generator initiates transmission under the timing commands generated by the synchronizer. In steady-state operation, the burst synchronizer tracks loop-back transmissions, adjusting them in small increments at time intervals slightly exceeding the round trip transmission delay, so that the station's timing relative to the reference UW remains as specified, thereby ensuring network synchronization.

Satellite Hardware Simulator

The AW satellite hardware simulator closely approximates the actual satellite. They are electrically identical except that the hardware simulator contains only a single channel. The hardware simulator connects the transmit station to the receive station. The transmit station takes the output of the TDMA data generator and generates the TDMA data burst at 14,387.5 MHz under the control of the burst synchronizer. From the Ku-band modulator the signal is routed to the AW satellite hardware simulator.

Prior to the satellite simulator, the transmit signal is filtered at 14.3875 GHz. Following this filter is a coupler which couples an adjacent channel 250 Mbps SQPSK signal of 14.1125 GHz to the 14.3875 GHz signal. This coupling allows the effect of adjacent channel interference to be simulated.

BER Test Results

The test results reported here fall into one of two categories: BER measurement or acquisition data. All BER data are normalized with respect to useful carrier power, as described in the Appendix. It is also an accepted practice to normalize the signal energy relative to available signal power. If this practice had been followed, all results quoted in this report would improve by approximately 0.5 dB.

Clock Frequency Offset

Figure 6 shows BER vs E_b/N_0 performance data for the complete communication link. In this figure, the clock frequency of the transmit station is offset without disturbing other system clocks; i.e., the receive station clock, satellite clock, and the RS clocks remain unchanged to provide maximum system stress. In Fig. 6, the theoretical BER curve is plotted to allow evaluation of system performance at a glance. The triangles indicate performance at no clock offset. Note that the I channel (Δ) outperforms Q(∇) by 0.5 dB. This imbalance can be the result of various causes but is most likely caused by a combination of imperfections, such as recovered carrier phasing error, I/Q detector imbalance, imperfections in the detection filter/baseband amplifier chain, decision timing offset, etc. As the clock is offset ± 2 kHz, no visible impact on error rate occurs in the I or Q channel. The key in the upper corner of the graph shows which symbol corresponds to the positive or negative offset, also differentiating the I and Q channels.

The implications of these data are that relatively inexpensive sources can be used in both the transmit and receive Earth stations without significant maintenance time for adjustment of oscillator frequency. Also, with a very

forgiving maintenance schedule, 2 kHz represents a frequency offset in excess of 10 pulses per min (ppm).

Input Frequency Error

The AW communication system operates via a satellite where spectral inversion takes place. The spacecraft local oscillator will drift as a function of in-orbit time, causing as much as 170 kHz frequency offset at end of life. While it is possible to lock the spacecraft oscillator to a stable, ground-based reference, current AW specifications require non-degraded performance without such a pilot signal. Our demodulator is designed to operate over a ±200 kHz frequency range. To test the frequency sensitivity of the demodulator, the input frequency to the upconverter in the AW satellite simulator was varied. The resulting data (Fig. 7) reveal immeasurable BER impact at a ±200 kHz frequency offset. A <0.25 dB variation of performance can be attributed to a number of possible causes, such as randomness of measurement error, small sample base, and change in operating temperature. Therefore, this design allows the utilization of the master frequency source onboard the AW satellite, without BER penalty. It further allows the utilization of relatively inexpensive LO/modulator frequency sources, in both the transmit and receive portions of the AW Earth stations.

Burst Sequencing

To evaluate the system performance when successive noncoherent bursts are received from different transmitters, the PLL lock point was slipped between each successive transmission. The carrier phase was advanced 90 and 180 deg, alternatively. To test the impact of phase change between bursts, testing with minimum guard times between bursts and transmit burst lengths would be ideal. The prototype system is constrained to transmit a maximum of 8 bursts per frame by memory size selection. Given this constraint, if only 10 symbols were transmitted 8 times in a 750 μsec frame, BER data would have required an unacceptably excessive test time, especially at reasonably low error rates. As a compromise, 8 bursts per frame were selected, with symbol lengths equal to 1023, 1022, 1022, 1022, 1022, 22, 22, and 22. The same sequence was used for lock-point evaluation and for finding the impact of sequencing.

In Fig. 8, the BER degradation with respect to theoretical was plotted for these cases. The Δ represents the case where the lock point is sequenced between each burst. The □ symbol indicates the average BER degradation averaged over all four lock points. One cannot observe a consistent advantage of one condition relative to the other, implying no measurable penalty due to sequencing. This conclusion is not surprising because the recovered carrier, as well as the recovered symbol timing, is quenched at the end of each burst. The ◇ symbol shows the BER performance measured utilizing the optimum lock point. This lock condition results in a performance improvement of approximately 0.2 dB, implying a small but measurable modulator and I/Q detector imbalance, respectively.

Uplink Noise

As shown in the Appendix, BER tests are typically taken by introducing calibrated noise at the receiver input. In most cases, this is realistic even for satellite signals because uplink E_b/N_0 exceed downlink E_b/N_0. Nevertheless, it is interesting to evaluate the effect of uplink noise on the overall system BER. To do so, we measured communication performance vs overall E_b/N_0 at various uplink E_b/N_0.

The effect of uplink noise is summarized in Fig. 9. To attempt to reduce the smearing generated by measurement errors, curves are drawn to the data points in Fig. 9. The solid line represents the case where all the noise is contributed by the downlink; the dotted line represents the case where the

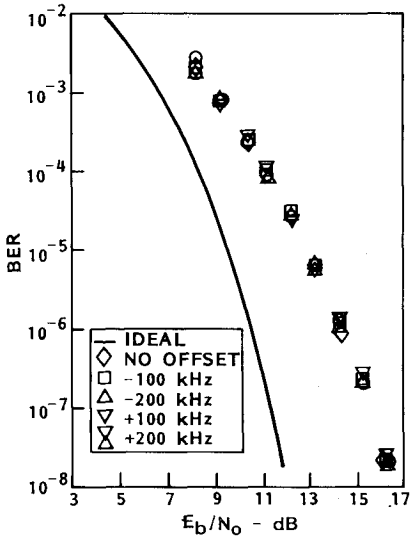

Fig. 7 Degradation to BER, function of input frequency offset.

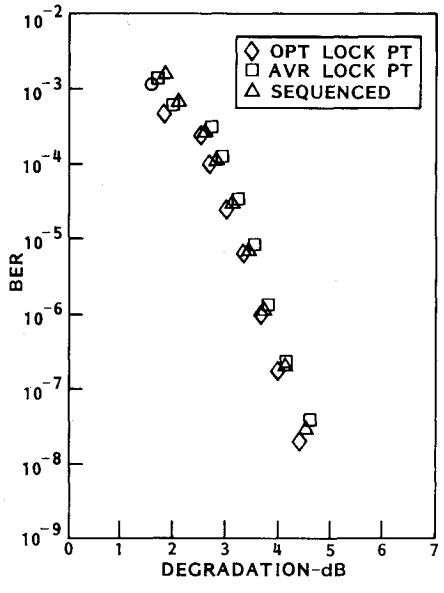

Fig. 8 Degradation to BER, function of sequencing between bursts.

downlink noise contribution is immeasurably small; i.e., all noise is contributed by the uplink. To ease comparison, the I and Q channel performances are combined. Little impact of uplink noise is observed at better than 10^{-4} error rates. As the E_b/N_0 of the uplink further degrades to below 10 dB, there seems to be as much as 0.5 dB excess BER penalty.

Acquisition Tests

Acquisition tests show that, without undue frequency stresses in the system, the RS is quickly acquired after station "turn on" at 4 dB E_b/N_0 in the actual configuration. Using the worst case (largest specified) frequency offset of ±170 kHz, rapid acquisition occurs between 6 and 7 dB E_b/N_0. In these tests, RS acquisition is defined as the finding of the RUW of either the primary or secondary RS and locking to it; i.e., entering into the steady-state tracking mode of the reference stations.

When the system is well tuned, acquisition occurs at as low as 4 dB E_b/N_0. The station can enter the communication network when the E_b/N_0 approaches 6 dB. Another statistic of interest is the E_b/N_0 at which the same station will drop out of the network. Test data shows that at 2.5 dB E_b/N_0, the mean time between loss of lock is approximately 1 min;

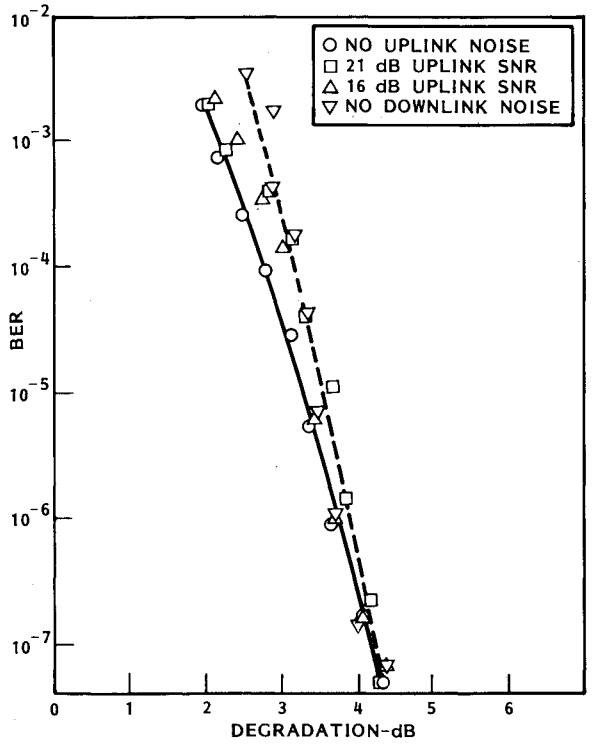

Fig. 9 Degradation to BER, function of uplink noise.

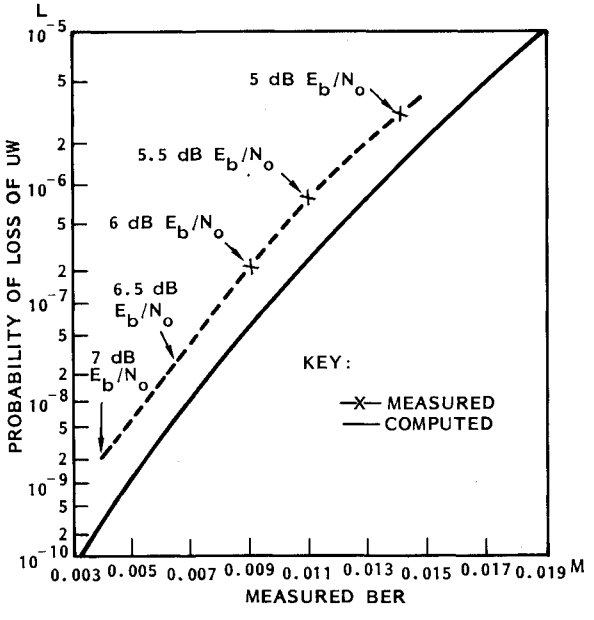

Fig. 10 Probability of UW loss function of BER.

at 3 dB, it is approximately 10 min; while at 3.5 dB, it exceeds 1 h. Unlike RS acquisition, this value is virtually independent of input frequency offset, since the demodulator AFC is already tracking. Hence, if the system operates at an E_b/N_0 as low as 9 dB, fades as deep as 6 dB are not likely to cause a station to drop from the TDMA network, even though it will experience a temporary increase of BER.

Comparison to Analysis

Prior to undertaking this development work, a number of detailed analysis and simulation tasks were performed on the modem and on the complete network. For example, the modem was designed to acquire symbol timing and carrier recovery in 60 symbols with a performance degradation of

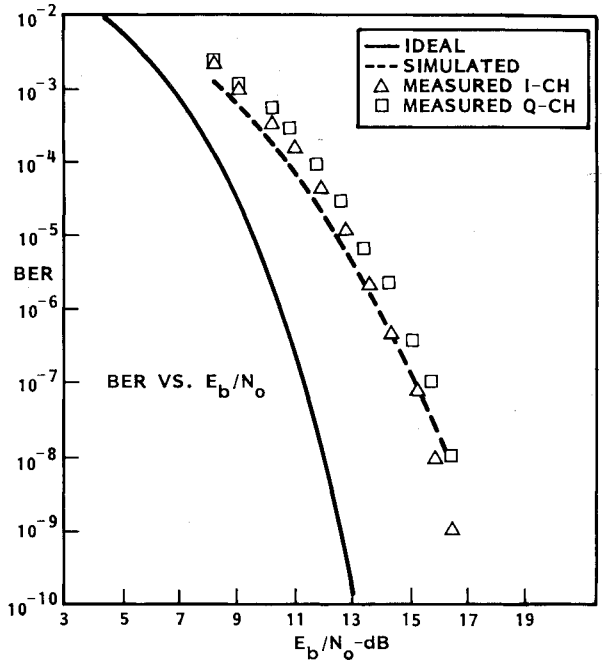

Fig. 11 BER performance, measured vs simulated.

less than 0.5 dB at the 61st symbol, relative to the nth symbol ($n \gg 61$). Subsequent measurements showed a degradation of approximately 0.2 dB.

Bit count integrity is lost in a TDMA system in one of two ways. A burst can be lost by missing the UW. Cycle slip or excessive noise can cause clock modulation, so that one bit is dropped or a nonexistent bit is read into the data buffer. For this type of TDMA modem, there is a tradeoff between fast carrier acquisition and cycle slipping at low values of E_b/N_0. Based on acquisition requirements, analysis showed that cycle slipping will be negligible to 6 dB E_b/N_0. For this reason, the modem was designed to operate down to 6.9 dB E_b/N_0, with a probability of a 10^{-8} data burst loss. Subsequent test results showed that the effects of cycle slipping can be ignored down to about 4.5 dB E_b/N_0, and the loss of burst probability of 10^{-8} is achieved at approximately 6.7 dB E_b/N_0.

In the absence of cycling slipping and other secondary effects, the probability of a burst loss is determined only by the probability of missing a UW; i.e., by the probability of exceeding the detection error threshold for the UW. This probability is displayed in Fig. 10, together with the measured performance. The measured results are extrapolated based on measurements at UW loss frequencies in the range of 3×10^{-6} to 2×10^{-7}. Statistical measurements at a frequency of 10^{-8} would be prohibitive in terms of measurement time. There is a 0.2 dB discrepancy between the computation and the measurement. This discrepancy can be due to calibration errors as well as a slight degradation of BER at the beginning of the burst, where the UW is located.

Prior to hardware development, the overall simulated communication link performance was published stating that the impact of carrier recovery could not be simulated at that time; therefore, it was ignored. Subsequent test data on the same communication link is shown in Fig. 11. The measured overall system performance is 0.5 dB worse than expected from the software simulation utilizing the TRW LINK computer program when that program ignores the carrier recovery penalty.[3]

Hardware measurements comparing recovered carrier and hardlined carrier performance shows that 0.25 dB can be allocated to carrier recovery penalty, resulting in 0.25 dB performance variation between software simulations for the complete system and actual hardware measurements.

Conclusion

The operational capability of a 250 Mbps TDMA link was demonstrated. The frame synchronizer was designed to track multiple RSs, transmit a large number of TDMA bursts per frame, receive nonoverlapping TDMA messages from various sources, and establish symbol timing for every received burst based on the position of a UW in that burst. The TDMA demodulator was designed to accept asynchronous burst, nominally separated by five symbols.

Test data show that the system operates at 250 Mbps, as expected from analysis performed as part of the design. Test results also verify that the system does not show undue sensitivity to frequency offset or other hardware imperfections. Stations can enter the network at E_b/N_0 as low as 6 dB; once acquired, they can stay in the network to approximately 3 dB E_b/N_0.

Appendix: BER Measurements

For wideband systems the noise spectral density is not really flat. Therefore, the measurement of BER requires knowledge of noise and signal powers and the various bandwidth constraints within the system. The technique to assess the BER performance of the demodulator unit includes the noise power measurement through a known filter bandwidth and detection filter characteristics. The resultant correction factor is applied to the measurements, thus increasing the accuracy of the reported data. Let σ^2 be the noise output spectrum of the demodulator, then:

$$\sigma^2 = \int S_n(f)\,|H(f)|^2 df$$

Similarly, the output spectrum (σ^2) is related to

$$\sigma^2 + N_0^{eq} \int |H(f)|^2 df$$

where $H(f)$ is the combined response of the internal demodulator filters (Fig. A1) and

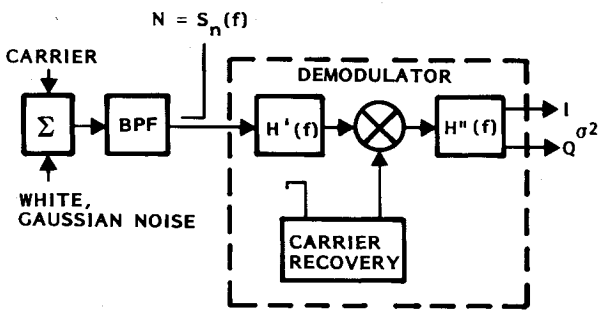

Fig. A1 BER calibration block diagram.

$$N_{MEAS} = \int S_n(f)\,df$$

is the actual noise power spectral density times the measurement bandwidth. Therefore, the E_b/N_0 per bit is

$$\frac{E_b}{N_0} = \frac{\text{signal power} \times \text{bit time}}{\text{noise power per bit}}$$

N_0^{eq} = equivalent flat spectral noise density

or

$$\frac{E_b}{N_0} = \frac{CT_{bit}}{N_0^{eq}}$$

Substituting for N_0^{eq}

$$\frac{E_b}{N_0} = \frac{CT_{bit}}{N_{MEAS}} K$$

where

$$K = \frac{\int S_n(f)\,df \int |H(f)|^2 df}{\int S_n(f)\,|H(f)|^2 df}$$

If $S_n(f)$ is flat and of very wide bandwidth relative to the detection bandwidth, then K becomes the equivalent noise bandwidth N_{BW}.

$$\frac{E_b}{N_0} = \frac{CT_{bit}}{N_{MEAS}/N_{BW}}$$

is the well-known expression for BER measurement at data rates where the noise spectral density is totally flat over the spectral occupancy of the signal.

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